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Automatic Extraction of an Equivalent Circuit from a TFT-LCD Unit Cell for LCD TV Application

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In this article, we present a novel scheme for automatic generation of an equivalent circuit for unit cell of LCD-TV. In order to automatically extract a circuit model, a computer program generates an electrical connectivity of resistors and capacitors from the layout information through a so-called pattern analysis with electrode and port information. Thereafter, the Ericksen-Leslie's equation and two types of Laplace's equation in the dielectric and conductor domain are solved by finite element method (FEM). Finally, we can obtain a resistive equivalent circuit and a capacitive equivalent circuit in an independent manner. For combining two types of independent equivalent circuits, we propose a node insertion algorithm which enables us to generate an equivalent RC circuit without increasing the capacitive elements.

Keywords: finite element method; liquid crystal display; simulation; SPICE model

I. INTRODUCTION

With today's improved color depth and increase in LCD-TV panel size, interconnect delay of bus lines and its effects have become a dominant factor in LCD-TV performance [1,2]. Therefore, an accurate pre-analysis on the electrical properties of bus lines in the LCD panel is critically important at the design and verification stage of a unit pixel. In addition, from the aspect of electrical analysis the knowledge of

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the accurate resistance and capacitance in the LCD panel is important to predict the degradation of color image caused by crosstalk, shading, flicker, and gray scale errors.

Since experimental measurements for extracting capacitance and resistance are difficult and time-consuming and sometimes impossible at all, there is a need for numerical calculation of resistance and capacitance. In order to compute the capacitance and resistance, Laplace's equation should be solved numerically over the charge-free region and the resistive region with the conductors providing boundary conditions [3]. Furthermore, since the liquid crystal material in TFT-LCD devices possess dielectric anisotropy, the rigorous three-dimensional numerical technique which can take the liquid crystal's dielectric anisotropy into account should be applied. Moreover, even though we calculated the resistance and capacitance using a numerical method, since the capacitance and resistance were calculated by an independent manner, these circuit elements should be combined as an equivalent circuit.

Therefore, in this paper, we undertook a study of an automatic extraction of an equivalent circuit from the layout of a TFT-LCD unit cell including the calculation of parasitic elements in its three-dimensional structure.

II. Extraction of Parasitics

We have used the energy method, which calculates capacitance and resistance values from the electric-field energy stored in the dielectrics and the power loss in the conductors, respectively. The electric-field energy (W_D) stored in dielectrics and the power loss (W_C) in the conductors at the given electric-field configuration are as follows:

$$W_D = \frac{1}{2}\int_D \overline{E} \cdot \varepsilon \overline{E} dV \tag{1}$$

$$W_C = \int_C \overline{E} \cdot \sigma \overline{E} dV \tag{2}$$

where, ε and σ are material constant, permittivity tensor and electrical conductivity, in particular, the dielectric anisotropy of liquid crystal is described by Eq. (3):

$$\varepsilon = \begin{bmatrix} \varepsilon_\perp + (\varepsilon_\perp - \varepsilon_\parallel)n_x^2 & (\varepsilon_\perp - \varepsilon_\parallel)n_x n_y & (\varepsilon_\perp - \varepsilon_\parallel)n_x n_z \\ (\varepsilon_\perp - \varepsilon_\parallel)n_y n_x & \varepsilon_\perp + (\varepsilon_\perp - \varepsilon_\parallel)n_y^2 & (\varepsilon_\perp - \varepsilon_\parallel)n_y n_z \\ (\varepsilon_\perp - \varepsilon_\parallel)n_z n_x & (\varepsilon_\perp - \varepsilon_\parallel)n_z n_y & \varepsilon_\perp + (\varepsilon_\perp - \varepsilon_\parallel)n_z^2 \end{bmatrix} \tag{3}$$

where, $\varepsilon_{\perp}$ and $\varepsilon_{\parallel}$ are transverse and longitudinal dielectric constant of liquid crystal, respectively. Further, n_i denotes the director of liquid crystal molecule with $(i = x, y, z)$.

For the calculations of three-dimensional electric-field and the director distribution, we applied a finite element technique to the integral form of Laplace's equation and the Ericksen-Leslie's equation, respectively.

From the Eq. (1), on the assumption that the problem has n electrodes, W_D can be expressed by the linear summation of parasitic capacitance $(C_{i,j})$:

$$W_D = \frac{1}{2}\sum_{i=1}^{n-1}\sum_{j=i+1}^{n} C_{i,j}U_{i,j}^2 \tag{4}$$

where, $U_{I,j}$ is the voltage difference between i-th electrode and j-th electrode.

Therefore, the values of the parasitic capacitances can be obtained by solving a linear system of equations with m unknowns containing the squares of the voltage differences ${}^kU_{i,j}$ and the respective field energies, ${}^kW_D$,

$$\begin{bmatrix} {}^1U_{1,2} & {}^1U_{1,3} & \dots & {}^1U_{n-1,n} \\ {}^2U_{1,2} & {}^2U_{1,3} & \dots & {}^2U_{n-1,n} \\ \vdots & \vdots & \ddots & \vdots \\ {}^mU_{1,2} & {}^mU_{1,3} & \dots & {}^mU_{n-1,n} \end{bmatrix} \cdot \begin{bmatrix} C_{1,2} \\ C_{1,3} \\ \vdots \\ C_{n-1,n} \end{bmatrix} = \begin{bmatrix} 2\cdot{}^1W_D \\ 2\cdot{}^2W_D \\ \vdots \\ 2\cdot{}^mW_D \end{bmatrix} \tag{5}$$

where, $m = {}_{\mathrm{n}}\mathrm{C}_2$ denotes the total number of parasitic capacitances. A set of $k = 1 \dots m$ linear independent vectors containing the squares of the voltage differences has to be created ensuring that the determinant of its matrix is non-zero, and the m energies ${}^kW_D$ of the respective field distributions are the quantities to be calculated by the finite element method.

In similar, on the assumption that the problem has N ports, W_C can be express by the linear summation of parasitic conductance $(G_{i,j})$ equal to the reciprocal of resistance, $({R_{i,j}}^{-1}$, and it is used to set up a linear system of equations for calculation of resistances:

$$W_C = \sum_{i=1}^{N-1}\sum_{j=i+1}^{N} G_{i,j}U_{i,j}^2 \tag{6}$$

$$\begin{bmatrix} {}^{1}U_{1,2} & {}^{1}U_{1,3} & \cdots & {}^{1}U_{n-1,n} \\ {}^{2}U_{1,2} & {}^{2}U_{1,3} & \cdots & {}^{2}U_{n-1,n} \\ \vdots & \vdots & \ddots & \vdots \\ {}^{m}U_{1,2} & {}^{m}U_{1,3} & \cdots & {}^{m}U_{n-1,n} \end{bmatrix} \cdot \begin{bmatrix} G_{1,2} \\ G_{1,3} \\ \vdots \\ G_{n-1,n} \end{bmatrix} = \begin{bmatrix} {}^{1}W_C \\ {}^{2}W_C \\ \vdots \\ {}^{m}W_C \end{bmatrix} \tag{7}$$

III. GENERATION OF EQUIVALENT CIRCUIT

In order to generate equivalent circuit model, firstly, a resistive equivalent circuit and a capacitive equivalent should be generated. Figure 1 illustrates a schematic view of an exemplary layout, Referring to Figure 1, the layout includes 3 conductors (A, B, C) which have 2 ports (1, 2 in A), 0 port, and 3 ports (3, 4, 5 in C), respectively. Figure 2 shows its resistive and capacitive equivalent circuit.

For the resistive equivalent circuit, the conductor containing m ports can be modeled as ${}_{m}C_2$ resistors. In similar, for the capacitive equivalent circuit, n conductors can be modeled as ${}_{n}C_2$ capacitors. Therefore, referring to the Figures 2(a) and 2(b), conductors A was transferred in to a resistor and the conductor C was transferred into 3 resistors, 3 conductors were transferred into 3 capacitors.

In order to generate RC equivalent circuit for the exemplary layout shown in Figure 1, the resistive and capacitive equivalent circuit should be combined because resistance and capacitance were calculated independently. Therefore, we used node insertion method based on node elimination method.

Figure 3 shows a schematic view illustrating the rule of node elimination about resistive elements [4].

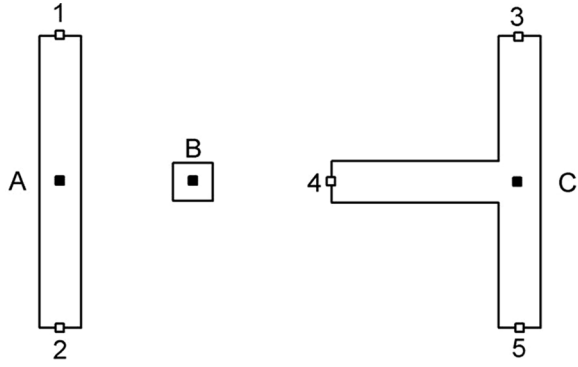

FIGURE 1 Schematic view of exemplary layout with electrical information.

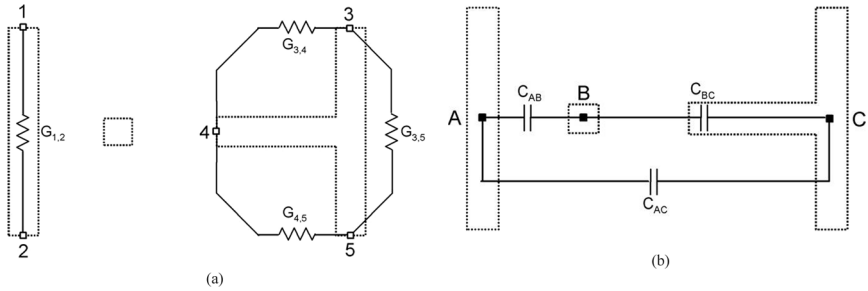

FIGURE 2 Schematic views of (a) resistive and (b) capacitive equivalent circuits.

Referring to Figure 3, conductance g_{mi} and g_{ni} can be merged into g_{mn}, and g_{mn} is described by Eq. (8),

$$g_{mn} = g_{mi}g_{ni} \Big/ \sum_{k=1}^{p} g_{ki}[4]. \tag{8}$$

From Eq. (8), the resistive and capacitive equivalent circuits shown in Figures 2(a) and 2(b) can be combined as shown in Figure 4.

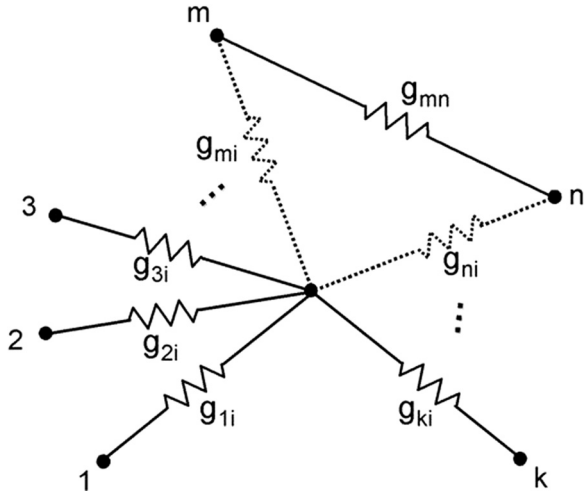

FIGURE 3 Schematic view illustrating the rule of node elimination about resistive element.

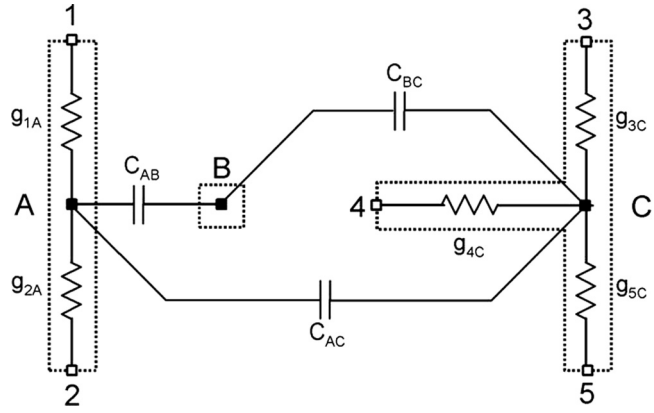

FIGURE 4 Merged equivalent circuit using node insertion algorithm.

Each conductance in Figure 4 is as follows:

$$g_{1A} = g_{1B} = \frac{1}{2} G_{1,2}, \tag{9}$$

$$g_{3C} = \sqrt{g_T \cdot \frac{G_{3,4} G_{3,5}}{G_{4,5}}},\ g_{4C} = \sqrt{g_T \cdot \frac{G_{3,4} G_{4,5}}{G_{3,5}}},\ g_{5C} = \sqrt{g_T \cdot \frac{G_{3,5} G_{4,5}}{G_{3,4}}}, \tag{10}$$

$$g_T = \frac{(G_{3,4} \cdot G_{3,5})^2 + (G_{3,4} \cdot G_{4,5})^2 + (G_{3,5} \cdot G_{4,5})^2}{G_{3,4} \cdot G_{3,5} \cdot G_{4,5}} + 2(G_{3,4} + G_{3,5} + G_{4,5}). \tag{11}$$

IV. APPLICATIONS

In this work, we have applied our method to the exemplary unit cell. Furthermore, a graphical input interface was developed to generate equivalent circuit automatically from the layout of unit cell. Figure 5 illustrate the layout of exemplary unit cell and its 3D structure. Referring to the Figure 5, the layout includes a total of 7 electrodes and 14 ports comprising two gate lines, two data lines, storage, pixel, and common electrodes. Furthermore, each one of data and gate lines, storage and pixel electrodes include two ports, respectively, while another one of data and gate lines include three ports and the common electrodes include no port. Therefore, the layout of the unit cell can be modeled by 10 resistances, 21 capacitances, and a TFT. We have used our FEM numerical solver to calculate the resistances and

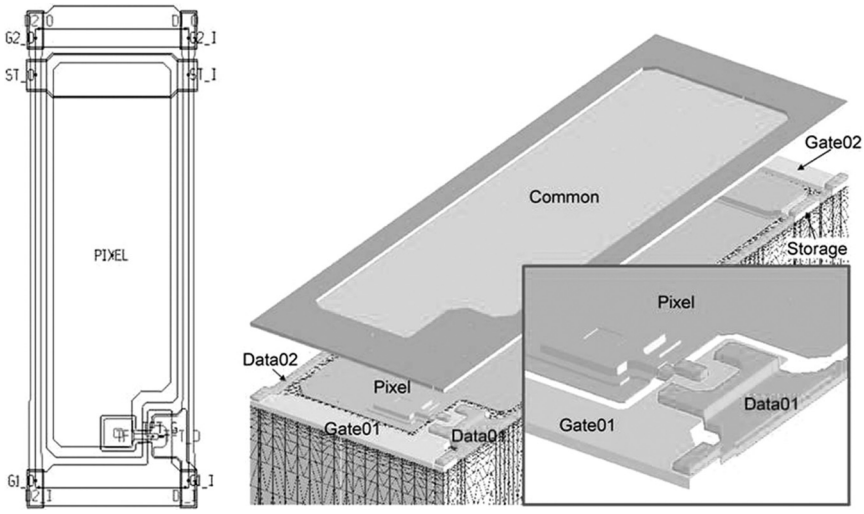

FIGURE 5 Schematic view illustrating the layout of exemplary unit cell of TFT-LCD and its 3D structure.

capacitances, and the calculated values were stored according to the convention of SPICE net-list for next-step circuit simulation and analysis. Figure 6 shows schematic view of the equivalent circuit of unit cell with some major parasitic elements.

To simulate the whole panel with the equivalent circuit of unit cell, however, an enormous CPU time as well as huge memory is required. Therefore, we divided SPICE net list of whole panel into many small-size lower-level net lists to overcome the issue of expensive CPU time with huge memory requirement. In this study, we constructed 768 net lists for the SPICE simulation with equivalent circuits of pixel arrays. The pixel employed in this work is a unit cell for 32″ TFT-LCD panel with a pixel size of 170×510 micrometers.

For modeling the liquid crystal (LC) capacitance of a pixel, a voltage dependent model was employed using the piece-wise voltage-controlled capacitor model. For modeling a thin-film transistor, the level 40 from the HP a-Si model was employed [5]. Table 1 shows a list of capacitance values employed in this work. The parametric values of the capacitances illustrated in Table 1 were obtained from the numerical simulation by our FEM solver.

It is assumed that the time duration of each frame is 16.7 ms while the pulse widths of a gate and data signals are 18.29 and 20.74 micro-second (μS), respectively. The root-mean-squared (RMS) value of a

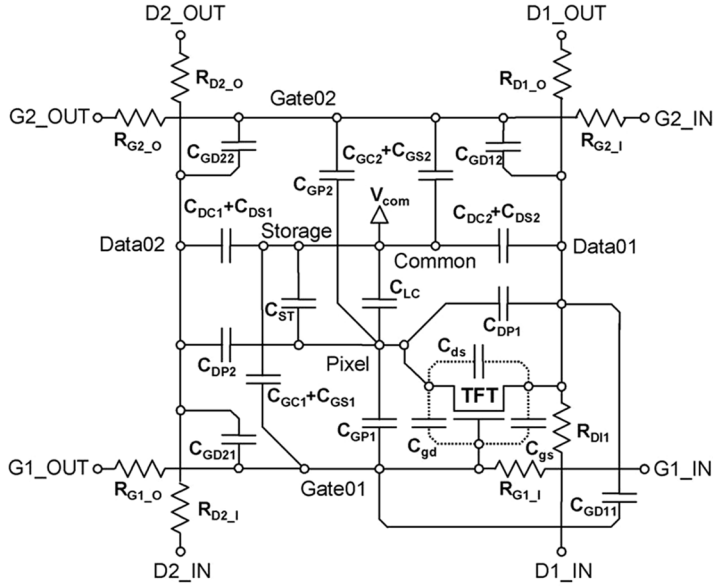

FIGURE 6 Schematic view of the equivalent circuit of unit cell with some major parasitic elements.

pixel voltage is obtained and then converted to an image data through the mapping of V-T and gamma curves. During the circuit simulation, the gate resistance was chosen to be 3.2 and 19.2 ohms while the data line resistance being 11.2 and 67.2 ohms.

Figure 7 is an original reference image with 1366×768 size having 8-bit color. The image quality of Figure 7 is HDTV while the gray-level of R, G, and B is 256. From the reference image shown in Figure 7, a gray-level was extracted from the V-T curve and a gamma correction curve. In this work, it is assumed that the gate line resistance for the worst case simulation was chosen to be 19.2 ohms. Figure 8 exhibits the simulated image taking into account all the resistance and capacitances in the model for the worst case.

TABLE 1 Capacitances of TFT-LCD Panel Used in the Simulation

Capacitor	Value [pF]	Capacitor	Value [pF]
Cst	0.64897	Cgdl	0.09547
Cdcl	0.07978	Cdc2	0.06672
Cdpl	0.04931	Cdp2	0.03924
Cgpl	0.00873	Cgp2	0.01037

FIGURE 7 Original reference image with 1366×768 size having 8-bit color.

In this simulation, the general column inversion was assumed. The gate voltage ranges from -6 to 30 V while the common voltage is set 6.5 V and the data voltage varies between 0 and 14 V. Referring to Figure 8, we can observe the shading effect and gray scale error induced by gate line delay in the simulated image of the panel. Furthermore, a vertical line crosstalk induced by driving with column line inversion is visible if we take a careful look at the simulated image. In Figure 8, the gray scale error is clearly depicted from the 520-th pixel to the last pixel, which seems to be due to the gate line delay.

Figure 9 exhibits a simulated image when the gate line resistance is to be 3.2 Ω with keeping other parameters unchanged. Referring to Figure 9, vertical line crosstalk and gray scale error seem to be

FIGURE 8 Simulated image taking into account all the resistance and capacitances in the model for the worst case.

FIGURE 9 Simulated image while the gate line resistance is 3.2 ohms with keeping other parameters unchanged.

alleviated with comparison to the image illustrated in Figure 8. The simulation reveals that the image quality can be adjusted either by the magnitude of the metal line or the species of material of the row-line interconnection, as mentioned earlier. As the number of pixel is increased, the gray scale error tends to be more pronounced due to the fact that the worst case panel has a greater gate line resistance

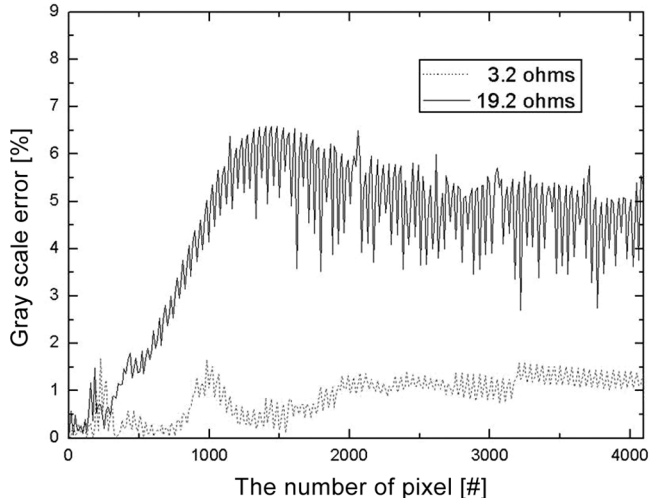

FIGURE 10 Schematic diagram illustrating the fluctuation caused by crosstalk.

than the improved panel. In Figure 10 is shown a schematic diagram illustrating the fluctuation caused by crosstalk.

V. CONCLUSION

In this article, we have proposed a method for automatic generation of an equivalent circuit for a unit cell of LCD-TV. In order to extract a circuit model of unit cell, we generated electrical connectivity of resistors and capacitors from the layout automatically by pattern analysis with electrical information comprising electrode and port information. In order to combine two type of independent resistive and capacitive equivalent circuit, we proposed node insertion algorithm. Thereafter, we calculated the parasitic elements by energy method with FEM. The output parasitics were stored according to the convention of SPICE net-list.

For application, electrical characteristics for 32″ HDTV TFT-LCD panel have been simulated by considering the voltage-dependent LC pixel capacitances and parasitic capacitances induced by adjacent gate and data lines. The simulation provides the visualization and also the valid prediction for the improvement of TFT-LCD panel. Various effects due to RC delay such as gray scale error were theoretically investigated, which implies a clue to design issue. The proposed technique can be applied to all types of TFT-LCD panel.

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